REMARKS

The claims remaining in the present application are Claims 37-52 and 71-79. Claim 43 has been amended. Claims 53-70 have been cancelled, without prejudice. Claim 79 has been added. No new matter has been added as a result of these amendments.

RESTRICTION/ELECTION

The rejection restricts the invention between:

> Group I, consisting of Claims 53-64; drawn to reordering instructions, and
> Group II, consisting of Claims 37-52 and 65-78, drawn to eliminating instructions.

Applicants elect, without traverse, Group II, drawn to eliminating instructions. Applicants have cancelled, without prejudice, Claims 53-64 from Group I and Claims 65-70 from Group II.

CLAIM REJECTIONS

35 U.S.C. §103

CLAIMS 37, 38, 42-52, and 65-78

Claims 37, 38, 42-52, and 65-78 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kahle et al., U.S. Patent No. 5,467,473 (hereinafter, Kahle) in view of Kreitzer et al., U.S. Patent No. 5,253,349 (hereinafter, Kreitzer). Claims 65-70 have been cancelled, without prejudice. Consequently, the rejection to Claims 65-70 is moot. The rejection to Claims 37, 38, 42-52, and 71-78 is respectfully traversed, for the following reasons.

Independent Claim 37 recites:

> A method of scheduling and executing instructions comprising:
> a) accessing a sequence of instructions comprising:
> a first memory operation that involves a first address range;

a second memory operation that involves at least a portion of said first address range; and

a third memory operation intervening said first and second memory operations, wherein it is not known whether said third memory operation involves an address within said first address range, wherein at least one of said first through third memory operations comprises a store operation;

b) eliminating said second memory operation from said sequence of instructions;

c) executing said sequence of instructions with said second memory operation eliminated; and

d) determining, during said executing, if said third memory operation involves an address within said first address range.

Independent Claim 37 recites an embodiment that specifically recites relationships between three instructions (memory operations). Limitations are recited as to the order of the instructions, eliminating the second memory operation from the sequence of instructions, and determining if the third memory operation involves an address of a memory operation of the first memory operation. Applicants respectfully assert that even if Kahle and Kreitzer were to be combined, the combination would teach or suggest the embodiment recited in Claim 37.

Kreitzer teaches the use of hardware for eliminating certain "type I dyadic instructions." More particularly, Kreitzer teaches that a write to memory is un-necessary when the value to be written to a memory location is the same as the value that currently exists at the location to be written (Kreitzer, col. 1, lines 11-25). Kreitzer provides circuitry to test whether the result obtained from executing the type I dyadic instruction equals the value already at the memory location to be written. If they are equal, then the memory write operation is eliminated. This shortens the execution time of type I dyadic instructions. (Applicants note that the type I dyadic instruction itself is not eliminated from a sequence of instructions.)

Kreitzer provides a hardware comparator circuit to accomplish the above. One input to the comparator is the result of executing the type I dyadic instruction far enough to

determine the value that is potentially going to be stored. The other input of the comparator is the operand originating from the memory location to be written. Thus, the comparator provides an instantaneous indication of whether the result of the (partial) execution of the instruction is identical to what is already stored in the location to be written (Kreitzer, col. 1, lines 51-58).

Kahle teaches a system that allows for out of order processing of instructions. Kahle's system seeks to enhance efficiency by delaying execution of store instructions. To increase efficiency, Kahle re-orders instructions by placing load instructions ahead of store instructions (Kahle, col. 3, 57-66). However, Kahle must determine if a re-ordering violation has occurred, due to previously executed load instructions. Kahle first re-orders instructions that comprise loads and stores. During execution of a store instruction, Kahle's system compares the addresses loaded from by previously executed load instructions with an address stored to by the presently executing store instruction. Kahle further compares positions in the sequence of instruction before the re-ordering of the presently executing store instruction with the load instructions. If the store and load instructions are to/from the same address, and if the store instruction occurs before the load instruction in the (original) program sequence, then a re-order violation has been detected (Kahle, Abstract).

To accomplish the above, Kahle teaches a "load instruction queue" for storing information related to recent load instructions. In particular, the load instruction queue stores the addresses from which each load instruction loaded, and the program numbers (i.e., location in the original program sequence) of each load instruction. Kahle further teaches means to compare the address to which a presently executing store instruction stores and its program number with those of load instructions in the load instruction queue (see e.g., Kahle Fig. 5).

Applicants respectfully assert that even if Kahle were to be combined with Kreitzer, the combination would not result in the claimed combination recited in Claim 1. That is, Applicants respectfully assert that if the hardware comparator taught by Kreitzer were to be combined with the load instruction queue and associated comparison means of Kahle, the result would not be the embodiment recited in Claim 37.

For the sake of argument, assume that of the three claimed instructions in Claim 37 two are load instructions in Kahle's load instructions queue and the other is the store instruction in Kahle that is being compared with the previously executed load instructions in the load instruction queue. In accordance with Kahle's teaching, the load instructions in the load instruction queue have already been executed, thus are not candidates for the claimed "eliminating a second memory operation from the sequence of instructions."

As the only instruction in Kahle that is a candidate for removal is Kahle's store instruction, to combine Kreitzer's hardware comparator with Kahle's queue would appear to the Applicants to require Kreitzer's hardware comparator to compare two operands of the store instruction (i.e., Kahle's store instruction that is being compared with the previously executed load instructions in the load instruction queue).

However, the result of this combination is not the embodiment claimed in Claim 37. Applicants have claimed in d) that during executing of the sequence of instructions the address of the third memory operation is tested an address within said first address range. In contrast, the combination of Kahle and Kreitzer does not teach or suggest any mechanism for testing the claimed third memory operation. This is because Kahle fails to teach or suggest a comparison between load instructions in the load queue. That is, Kahle teaches comparing addresses of the presently executing store instruction with previously executed load instructions. However, as Applicants have previously noted, it would

appear that the presently executing store instruction in Kahle does not read on either of the first or third claimed instructions. Thus, bearing in mind the claimed relationships between the first, second, and third memory operations, Kahle's contribution to the combination of Kahle an Kreitzer fails to teach or suggest, "during executing of the sequence of instructions the address of the third memory operation is tested an address within said first address range."

Furthermore, Kreitzer's contribution to the combination of Kahle and Kreitzer fails to teach or suggest, "during executing of the sequence of instructions the address of the third memory operation is tested an address within said first address range." This is because Kreitzer's comparison involves operands of a single instruction. However, the presently discussed limitation involves a comparison of addresses of different instructions. Thus, even if Kreitzer's teaching were to be combined with Kahle's teaching, the embodiment claimed in Claim 37 would not be realized.

Applicants further traverse the rejection to Claim 37 for the following reason. Claim 37 recites, "eliminating said second memory operation from said sequence of instructions." By this, the Applicants mean that the second instruction is eliminated from the sequence of instructions. Kreitzer fails to teach or suggest eliminating an instruction from a sequence of instructions, as claimed. Rather, Kreitzer teaches eliminating a memory store. However, the instruction must be partially executed in order to produce one of the inputs to Kreitzer's comparator. Thus, in accordance with Kreitzer's teaching, the instruction itself remains in the sequence of instructions, in contrast to the Applicants' claimed eliminating of the second memory operation (instruction) from said sequence of instructions.

Kahle fails to remedy this deficiency in Kreitzer, in that Kahle teaches reordering instructions as opposed to eliminating instructions. Therefore, the combination of Kahle and

Kreitzer fails to teach or suggest the limitation of, "eliminating said second memory operation from said sequence of instructions," as claimed.

For the foregoing reasons, Independent Claim 37 is not rendered obvious over Kahle in view of Kreitzer. Therefore, Applicants earnestly request allowance of Claim 37.

CLAIM 45

Independent Claim 45 recites:

> A method of scheduling and executing instructions comprising:
> a) accessing a sequence of instructions comprising:
> a first load instruction that loads from a first address range;
> a second load instruction that loads from said first address range; and
> a store instruction intervening said first and second load instructions,
> wherein it is not known whether said store instruction stores to an address within said first address range;
> b) eliminating said second load instruction from said sequence of instructions;
> c) executing said sequence of instructions without said second load instruction; and
> d) determining, during said execution, if said store instruction stores to an address within said first address range.

Independent Claim 45 recites an embodiment in which a sequence of instructions comprises two load instructions and a store instruction. The embodiment in Claim 45 is not of the same scope as the embodiment in Claim 37; however, the reasoning discussed in the response to Claim 37 is applicable to the limitations of Claim 45. Thus, Claim 45 is respectfully believed to be allowable for the same rationale as discussed in the response to Claim 37.

Applicants further traverse the rejection to Claim 45 on the grounds that Kreitzer teaches eliminating a memory operation associated with a store instruction. However, the embodiment recited in Claim 45 claims eliminating a load instruction from the sequence of instructions. Furthermore, Kreitzer teaches eliminating a memory operation associated with a store instruction, but not eliminating the instruction itself from a sequence of instructions, as

the Applicants have claimed. Therefore, Kreitzer fails to teach or suggest the claimed limitation of, "eliminating said second load instruction from said sequence of instructions."

Kahle fails to remedy this deficiency in Kreitzer in that Kahle teaches reordering instructions as opposed to eliminating instructions. Therefore, the combination of Kahle and Kreitzer fails to teach or suggest, "eliminating said second memory operation from said sequence of instructions," as claimed.

Thus, Applicants respectfully assert that the combination of Kahle and Kreitzer fails to teach or suggest the embodiment recited in Claim 45. Consequently, Applicants respectfully request allowance of Claim 45.

CLAIM 49

Independent Claim 49 recites:

> A method of scheduling and executing instructions comprising:
> a) accessing a sequence of instructions comprising:
> a first store instruction to a first address range;
> a second store instruction to said first address range; and
> a load instruction intervening said first and second store instructions, wherein it is not known whether said load instruction involves said first address range;
> b) eliminating said first store instruction from said sequence of instructions;
> c) executing said sequence of instructions with said first stored instruction removed; and
> d) determining, during said executing, if said load instruction involves an address in said first address range.

Independent Claim 49 recites an embodiment in which a first store instruction is eliminated from a sequence of instructions. Applicants traverse the rejection to Claim 49 on the grounds that Kreitzer teaches eliminating a memory operation associated with a store instruction. However, the store instruction itself is not eliminated from the sequence of instructions, according to Kreitzer. This is because the store instruction in Kreitzer must be partially executed to formulate the result to potentially be stored, such that one of the inputs to Kreitzer's comparator is determined.

In contrast, the embodiment recited in Claim 49 claims eliminating a store instruction itself from the sequence of instructions. Therefore, Kreitzer fails to teach or suggest the claimed limitation of, "eliminating said store instruction from said sequence of instructions."

Kahle fails to remedy this deficiency in Kreitzer in that Kahle teaches reordering instructions as opposed to eliminating instructions. Therefore, the combination of Kahle and Kreitzer fails to teach or suggest, "eliminating said second memory operation from said sequence of instructions," as claimed.

Thus, Applicants respectfully assert that the combination of Kahle and Kreitzer fails to teach or suggest the embodiment recited in Claim 49. Consequently, Applicants respectfully request allowance of Claim 49.

CLAIM 71

Independent Claim 71 recites:

> A method of scheduling and executing instructions comprising:
> a) accessing a sequence of instructions comprising:
> a first store instruction that stores to a first address range;
> a load instruction that loads from said first address range; and
> a second store instruction intervening said first store instruction and said load instruction, wherein it is not known whether said second store instruction stores to an address within said first address range;
> b) eliminating said load instruction from said sequence of instructions;
> c) executing said sequence of instructions without said load instruction; and
> d) determining, during said execution, if said second store instruction stores to an address within said first address range.

Claim 71 recites an embodiment in which a sequence of instruction comprises two store instructions and a load instruction. Claim 71 recites that the load instruction is eliminated from the sequence of instructions.

Applicants traverse the rejection to Claim 71 on the grounds that Kreitzer teaches eliminating a memory operation associated with a store instruction. However, the embodiment recited in Claim 71 claims eliminating a load instruction from the sequence of instructions. Therefore, Kreitzer fails to teach or suggest the claimed limitation of, "eliminating said second load instruction from said sequence of instructions."

Kahle fails to remedy this deficiency in Kreitzer in that Kahle teaches reordering instructions as opposed to eliminating instructions. Therefore, the combination of Kahle and Kreitzer fails to teach or suggest the claimed limitation of, "eliminating said second memory operation from said sequence of instructions," as claimed.

Applicants further traverse the rejection to Claim 71 on the grounds that Kreitzer teaches eliminating a memory operation associated with a store instruction. However, the instruction itself is not eliminated from the sequence of instructions, according to Kreitzer. This is because the instruction in Kreitzer must be partially executed to formulate the result to potentially be stored, such that one of the inputs to Kreitzer's comparator is determined.

In contrast, the embodiment recited in Claim 45 claims eliminating an instruction itself from the sequence of instructions. Therefore, Kreitzer fails to teach or suggest the claimed limitation of, "eliminating said load instruction from said sequence of instructions."

Kahle fails to remedy this deficiency in Kreitzer in that Kahle teaches reordering instructions as opposed to eliminating instructions. Therefore, the combination of Kahle and Kreitzer fails to teach or suggest the claimed limitation of, " eliminating said load instruction from said sequence of instructions," as claimed.

Thus, Applicants respectfully assert that the combination of Kahle and Kreitzer fails to teach or suggest the embodiment recited in Claim 71. Consequently, Applicants respectfully request allowance of Claim 71.

CLAIM 75

Independent Claim 75 recites:

> A method of scheduling and executing instructions comprising:
> a) accessing a sequence of instructions comprising:
> a load instruction that loads from a first address range;
> a first store instruction, wherein it is not known whether said first store instruction stores to an address within said first address range;
> a second store that stores to said first address range, wherein said first store instruction intervenes said load instruction and said second store instruction;
> b) eliminating said second store instruction from said sequence of instructions;
> c) executing said sequence of instructions without said second store instruction; and
> d) determining, during said execution, if said first store instruction stores to an address within said first address range.

Claim 75 recites an embodiment in which a store instruction is eliminated from a sequence of instructions. Applicants traverse the rejection to Claim 75 on the grounds that Kreitzer teaches eliminating a memory operation associated with a store instruction. However, the store instruction itself is not eliminated from the sequence of instructions, according to Kreitzer. This is because the store instruction in Kreitzer must be partially executed to formulate the result to potentially be stored, such that one of the inputs to Kreitzer's comparator is determined.

In contrast, the embodiment recited in Claim 75 claims eliminating a store instruction itself from the sequence of instructions. Therefore, Kreitzer fails to teach or suggest, "eliminating said store instruction from said sequence of instructions," as claimed.

Kahle fails to remedy this deficiency in Kreitzer in that Kahle teaches reordering instructions as opposed to eliminating instructions. Therefore, the combination of Kahle and

Kreitzer fails to teach or suggest, "eliminating said second memory operation from said sequence of instructions," as claimed.

Thus, Applicants respectfully assert that the combination of Kahle and Kreitzer fails to teach or suggest the embodiment recited in Claim 75. Consequently, Applicants respectfully request allowance of Claim 75.

CLAIMS 38, 42-44, 46-48, 50-52, 72-74, and 76-78

Dependent Claims 38, 42-44, 46-48, 50-52, 72-74, and 76-78 depend from Independent Claims 37, 45, 49, 71, and 75, which are believed to be allowable for the foregoing reasons. Therefore, dependent Claims 38, 42-44, 46-48, 50-52, 72-74, and 76-78 are believed to be allowable.

Dependent Claims 38, 43-44, 47-48, 51-52, 71, 74, and 77-78 are believed to be allowable for the following additional reasons.

CLAIMS 38, 47, 51, 71, 77

Dependent Claim 38 recites:

> The method of Claim 37, further comprising, prior to said executing said sequence of instructions, adding information to said third memory operation to allow determination of said first address range.

Dependent Claim 38 recites an embodiment in which information is added to the third memory operation itself to allow determination of the first address range. Thus, information is added to, and becomes a part of, the instruction itself.

The rejection refers to Kahle at col. 1, lines 45-48 when addressing Claim 38. Applicants note that this passage is describing U.S. Patent No. 4,630,195. Applicants respectfully assert that U.S. Patent No. 4,630,195 fails to teach or suggest the claimed

adding of information to an instruction to allow determination of an address range, as claimed. Rather, U.S. Patent No. 4,630,195 describes stored tags and tag registers in which information is stored. As Kahle summarizes U.S. Patent 4,630,195, "a tag is stored to identify a register in which data is stored (Kahle, col. 1, lines 45-47). While U.S. Patent No. 4,630,195 may teach comparing a data transfer to the stored tags, Applicants do not understand U.S. Patent No. 4,630,195 to teach or suggest the claimed limitation of, "adding information to said third memory operation to allow determination of said first address range."

The rejection also refers to Kahle at col. 9, lines 16-22 when addressing Claim 38. This passage of Kahle teaches marking load instructions that are executed out of order, such that if the need arises to re-execute instructions due to a scheduling violation, only store instructions that were incorrectly executed are re-executed. However, this passage fails to teach or suggest the claimed limitation of, "allowing determination of said first address range."

For the foregoing reasons neither Kahle nor U.S. Patent No. 4,630,195 teach or suggest the embodiment recited in Claim 38.

Kreitzer fails to remedy this deficiency in Kahle (and U.S. Patent No. 4,630,195) in that Kreitzer fails to teach or suggest, "adding information to said third memory operation to allow determination of said first address range," as claimed.

For the foregoing reasons, dependent Claim 38 is respectfully believed to be allowable over the cited art.

Dependent Claim 47 recites:

> The method of Claim 46, wherein said b) further comprises adding a flag to said store instruction to indicate said protection register.

Dependent Claim 47 is believed by Applicants to be allowance for the reasons discussed in the response to Claim 38.

Dependent Claims 51, 71, 77 recite limitations that are similar to Claim 47. Dependent Claims 51, 71, 77 are believed by Applicants to be allowance for the reasons discussed in the response to Claim 38.

CLAIM 43

Dependent Claim 43 recites:

> The method of Claim 42, wherein:
> said sequence of instruction comprises a fourth memory operation that is in said sequence of instructions after said first memory operation; and
> further comprising adding information to said fourth memory operation that allows said fourth memory operation to execute without exception even if said fourth memory operation involves said first address range (emphasis added).

The rejection cites col. 1, lines 45-48 of Kahle in support of the rejection of Claim 43. However, as Applicants have discussed in the response to Claim 38, this passage of Kahle (as well as U.S. Patent No. 4,630,195) fails to teach or suggest the claimed adding information to an operation.

Next, the rejection asserts that Kahle at col. 6, lines 1-13 teaches limitations of Claim 43. Applicants respectfully assert that Kahle fails to teach or suggest the limitations of Claim 43 in this passage or elsewhere. Rather than teaching the claimed "adding information to said fourth memory operation that allows said fourth memory operation to execute without exception even if said fourth memory operation involves said first

address range," this passage of Kahle teaches simultaneously executing two instructions (see e.g., Kahle col. 5, lines 63-67).

Kreitzer fails to remedy this deficiency in Kahle (and U.S. Patent No. 4,630,195) in that Kreitzer fails to teach or suggest, "adding information to said fourth memory operation that allows said fourth memory operation to execute without exception even if said fourth memory operation involves said first address range," as claimed.

For the foregoing reasons, dependent Claim 43 is respectfully believed to be allowable over the cited art.

CLAIM 44

Dependent Claim 44 recites:

The method of Claim 37, wherein said first and second memory operations would be safely reducible to a single memory operation if said third memory operation were not intervening.

Dependent Claim 44 incorporates the limitations of Independent Claim 37 and adds further to those limitations. The rejection states that Claim 44 is rejected for similar reasons as stated by the rejection in Claim 37. The reasons stated by the rejection in Claim 37 are not understood by the Applicant to be pertinent to the limitations of Claim 44. Applicants respectfully request that the Examiner specifically point out where the cited art teaches or suggests the limitations of Claim 44. As the rejection has failed to discuss the limitations of Claim 44, or similar limitations, Applicants respectfully assert that the rejection to Claim 44 fails to establish a prima fascia case for obviousness under 35 U.S.C. §103. Consequently, Applicants request the allowance of Claim 44.

CLAIMS 48, 52, 74, 78

Claim 48 recites:

> The method of Claim 45, wherein said b) further comprises changing said first load instruction to a load and protect instruction.

Claim 48 recites an embodiment in which, as a part of eliminating the second load instruction from the sequence of instructions, the first load instruction is changed to a load and protect instruction. The passages cited by the rejection do not teach or suggest changing a load instruction to another type of load instruction, as the Applicants have claimed. Rather, the cited passage (col., 6, lines 42-52) simply describes three different queues. One queue is for load instructions and the other two are for store instructions. Thus, Applicants note that only one of the queues is for load instructions. Applicants have previously discussed the load queue as being for storing load instructions that have executed. Thus, the cited passage provides no teaching or suggestion of the claimed limitation of, "changing a load instruction to a load and protect instruction."

Kreitzer fails to remedy this deficiency in Kahle in that Kreitzer fails to teach or suggest, "changing said first load instruction to a load and protect instruction," as claimed. For the foregoing reasons, Claim 49 is respectfully believed to be allowable over the Kahle in view of Kreitzer.

Dependent Claims 52, 74, and 78 recite limitations that are similar to Claim 48. Claims 52, 74, and 78 are respectfully believed to be allowable for at least the reasons discussed in the response to Claim 48.

CLAIMS 39-41

Claims 39-41 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kahle in view of Kreitzer, and in further view of Thayer et al., U.S. Patent No. 6,173,366 (hereinafter, Thayer). The rejection respectfully traversed, for the following reasons.

Claim 39 recites:

> The method of Claim 38, wherein said information comprises a mask allowing determination of which of a plurality of registers hold protected addresses.

Claim 39 further limits the "information that is added to the third memory operation" that is recited in Claim 38. Claim 39 recites that the information (added to the memory operation or instruction) comprises a mask allowing determination of which of a plurality of registers hold protected addresses. Thus, the mask recited in Claim 39 is a part of the instruction (memory operation). For the reasons discussed in the response to Claim 38, neither Kahle nor Kreitzer, alone or in combination, teach or suggest the claimed "information added to the instruction comprising a mask allowing determination of which of a plurality of registers hold protected addresses."

Thayer fails to remedy this deficiency in Kahle and Kreitzer in that Thayer fails to teach or suggest the claimed "information added to the instruction comprising a mask allowing determination of which of a plurality of registers hold protected addresses." This is because Thayer fails to teach or suggest adding information to an instruction. Rather Thayer teaches registers for holding masks, etc. (see, e.g., Thayer, col. 24, lines 36-40).

Claims 40-41 depend from Claim 39, which is believed to be patentable over Kahle in view of Kreitzer, and in further view of Thayer. Therefore, Claims 40-41 are respectfully believed to be allowable.

NEW CLAIM

Claim 79 has been added. Claim 79 depends from Claim 75, which is believed to be allowable for reasons above. Therefore, Claim 79 is believed to be allowable over the cited art. Consequently, Applicants earnestly request allowance of Claim 79.

CONCLUSION

It is respectfully submitted that Claims 37-52 and 71-79 are neither taught nor suggested by the cited references and, therefore, allowance of Claims 37-52 and 71-79 is earnestly solicited.

Should the Examiner have a question regarding the instant amendment and response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Dated: 2/20, 2004

Ronald M. Pomerenke
Registration No. 43,009

Address: WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, California 95113

Telephone: (408) 938-9060 Voice
(408) 938-9069 FAX